Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTION:**

1. **N. OE**
2. **1Q**
3. **1D**
4. **2D**
5. **2Q**
6. **3Q**
7. **3D**
8. **4D**
9. **4Q**
10. **GND**
11. **LE**
12. **5Q**
13. **5D**
14. **6D**
15. **6Q**
16. **7Q**
17. **7D**
18. **8D**
19. **8Q**
20. **VCC**

**.098”**

**.064”**

**13 12 11 10 10 9**

**8**

**7**

**6**

**5**

**4**

**14**

**15**

**16**

**17**

**18**

**19 20 20 1 2 3**

**HCT**

**373 G**

**MASK**

**REF**

**NOTE: Bond Pin/Pad #20 First**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004” X .004”**

**Backside Potential:**

**Mask Ref: HCT373 G**

**APPROVED BY: DK DIE SIZE .064” X .098” DATE: 8/26/21**

**MFG: TEXAS INSTRUMENTS THICKNESS .025” P/N: 54HCT373**

**DG 10.1.2**

#### Rev B, 7/1